REMARKS

The applicants appreciate the Examiner's thorough examination of the Application and request reexamination and reconsideration of the Application in view of the following remarks.

Claims 31-40 and 65-74 have been allowed. Additionally, claims 4, 5, 7, 18, 19, 21-23, 25, 26 and 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicants herein add claims 75-80 that correspond to claims 4, 5, 7, 19, 26 and 45 rewritten in independent form. Applicants have also amended claims 17 and 24 to incorporate the features of claims 18 and 25, respectively, to place claims 17, 18 and 21-23 in condition for allowance. Applicants would like to thank the Examiner for the indication of allowable subject material.

The Examiner rejects claims 1-3, 6, 12, 17, 24, 41-44, 50, 55, and 60 under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 4,829,236 to Brenardi *et al.* Applicants have amended claims 1, 12, 17, 24, and 41, and cancelled claims 2-6, 18-19, 25-26, 42-44 and 55-64 to better define the invention. Applicants have amended claims 7, 22-23 and 45 to correct claim dependencies.

Brenardi *et al.* shows a digital-to-analog calibration system that uses multiplier/accumulator circuit (MAC) 58 to modify digital data according to the function $y = mx + b$. To accomplish this, Brenardi *et al.* uses gain and offset coefficients stored in RAMs 44 and 46 to calibrate data. Brenardi *et al.*, however, does not teach, disclose or suggest a digital calibration circuit that includes a memory to store zero scale and full scale coefficients to adjust the end points of a digital-to-analog converter.

Claim 1 as amended, of the subject application recites: "An integrated programmable digital calibration circuit and digital to analog converter comprising: a digital to analog converter (DAC); and a digital calibration circuit including a memory for storing predetermined end point coefficients of said digital to analog converter transfer function, said end point coefficients including a zero scale and a full scale coefficient; and an arithmetic logic unit for applying the end point coefficients to the DAC input signal to adjust the end points of said DAC" (emphasis added). As noted above, Brenardi *et al.* does not teach, disclose or suggest a digital calibration circuit that includes a memory to store zero scale and full scale coefficients. Independent claims 12, 31, 36, 41, 50, 65, 70, 77 and 80 also include similar features that distinguish over Brenardi *et al.*

Claims 8-11, 13-16, 20, 27-30, 46-49, 51-54, 56-59 and 61-64 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Brenardi *et al.* in view of U.S. Patent No. 6,191,715 to Fowers *et al.* Since each of these claims depends from one of pending independent claims 1, 12, 17, 24, 31, 36, 41, 45, or 50, or has been cancelled, each of these claims which are pending are allowable for at least the reasons described above, and are further patentable because they include one or more additional features that distinguish over the prior art.

If for any reason this Response is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned, or his associates, collect in Waltham, Massachusetts, at (781) 890-5678.

Respectfully submitted,

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